WHAT IS CLAIMED IS:

1. A memory system having a module mounted with a plurality of memory circuits, and a controller for controlling said plurality of memory circuits, wherein said module is mounted with at least one buffer connected to said controller via data wiring for data transmission, and said buffer and said plurality of memory circuits are connected to each other via internal data wiring in said module.

2. A memory system according to claim 1, wherein said module is mounted with a plurality of buffers, and said plurality of buffers are connected to said controller via said data wiring.

3. A memory system according to claim 1 or 2, wherein said buffer is further connected to said controller via command/address wiring and clock wiring.

4. A memory system according to claim 3, wherein said buffer is connected to said memory circuits via internal command/address wiring and internal clock wiring corresponding to said command/address wiring and said clock wiring, respectively.

5. A memory system according to claim 4, wherein said internal command/address wiring and said internal clock wiring are commonly used for said memory circuits.

6. A memory system according to claim 1, wherein each of said memory circuits is a DRAM, and data is transmitted/received bidirectionally in said data wiring between said controller and said buffer.

7. A memory system having a plurality of modules each mounted with a plurality of memory circuits, and a controller for controlling the memory circuits of said plurality of modules, wherein each of said modules is provided with at least one buffer, and the buffer of each module is connected to the buffer

of another module and/or said controller via data wiring for data transmission.

8. A memory system according to claim 7, wherein the buffer of each module is connected to the buffer of another module and/or said controller via command/address wiring and clock wiring.

9. A memory system according to claim 7, wherein said data wiring forms a daisy chain by connecting the buffers of said plurality of modules and said controller in cascade.

10. A memory system according to claim 7, wherein each of said buffers of said plurality of modules is directly connected to said controller via said data wiring.

11. A memory system according to claim 10, wherein each of said buffers of said plurality of modules is further directly connected to said controller via command/address wiring and clock wiring.

12. A memory system according to claim 11, further comprising buffers provided on other modules and each connected to one of said buffers in cascade via data wiring, command/address wiring, and clock wiring.

13. A memory system according to claim 8, wherein said memory circuits of each module are grouped into a plurality of ranks, and the memory circuits, belonging to the same rank, of said plurality of modules are simultaneously accessible.

14. A memory system according to claim 12, wherein a data transmission speed on said data wiring is higher than a data transmission speed on internal data wiring between said buffer and each of said memory circuits on each module.

15. A memory system according to claim 14, wherein transmission speeds on said command/address wiring and said clock wiring are higher than transmission speeds on internal command/address wiring and internal clock wiring, corresponding to said command/address wiring and said clock wiring, between said buffer and said memory circuits on each module.

16. A memory system according to claim 14, wherein data for the buffers of said plurality of modules are transmitted in said data wiring in the form of a packet, and said buffers separate said data in the form of the packet.

17. A memory system according to claim 15, wherein commands/addresses and clocks for the buffers of said plurality of modules are transmitted in said command/address wiring and said clock wiring in the form of packets, and each of said buffers has a function of separating said commands/addresses and dividing said clocks in frequency.

18. A memory system having a module mounted with a buffer and a memory circuit connected to said buffer, and a memory controller connected to said buffer on said module, wherein a transmission speed between said memory controller and said buffer is higher than a transmission speed between said buffer on said module and said memory circuit connected to said buffer.

19. A memory system according to claim 18, wherein a plurality of modules each having said buffer and said memory circuit are provided, and said buffers of the respective modules are connected in turn in cascade relative to said memory controller via data wiring, command/address wiring, and clock wiring, and wherein said memory circuit and said buffer are connected to each other on each module via internal data wiring, internal command/address wiring, and internal clock wiring, and transmission speeds on said data wiring, said command/address wiring, and said clock wiring are higher than transmission speeds on said internal data wiring, said internal command/address wiring, and said internal clock wiring.

20. A memory system according to claim 19, wherein said memory circuit of each module is a DRAM, data phase signals are transmitted bidirectionally between said buffer and said DRAM on each module at timing that avoids collision therebetween, and each of said DRAM and said buffer produces internal clocks based on the received data phase signal and performs reception/transmission of data according to said internal clocks.

21. A data transmission method for transmitting/receiving data bidirectionally between a first and a second device, said first device receiving data according to first internal clocks, and said second device receiving data according to second internal clocks, wherein a first and a second data phase signal are continuously transmitted bidirectionally on the same wiring between said first and second devices at timing that avoids collision therebetween, said first device refers to timing of said first data phase signal to thereby transmit data to said second device, while said second device refers to timing of said second data phase signal to thereby transit data to said first device.

22. A data transmission method according to claim 21, wherein said second device produces said second internal clocks according to the received first data phase signal and receives the data from said first device according to said second internal clocks, while said first device produces said first internal clocks according to the received second data phase signal, produces said second data phase signal according to said first internal clocks, and receives the data from said second device according to said first internal clocks.

23. A data transmission method according to claim 21, wherein said first device suppresses said first data phase signal outputted from said first device from said first and second data phase signals transmitted bidirectionally, while said second device suppresses said second data phase signal outputted from said second device in said first and second data phase signals transmitted bidirectionally.

24. A data transmission method according to claim 21, wherein said first and second devices are a buffer and a DRAM, respectively, and said DRAM is given external clocks and produces said second internal clocks based on said external clocks and said received first data phase signal.

25. A data transmission method according to claim 21, wherein said first and second devices produce said first and second internal clocks from said second and first data phase signals using DLLs.

26. A data transmission system for transmitting/receiving data between a first and a second device, wherein a transmission side of said first and second devices has means for transmitting, upon transmission of said data, a data phase signal representing a predetermined phase of said data continuously irrespective of transmission of said data, and a reception side of said first and second devices has means for reproducing internal clocks of said reception side based on said data phase signal and receiving said data according to the reproduced internal clocks.

27. A data transmission system for transmitting/receiving data bidirectionally between a first and a second device, wherein each of said first and second devices has transmission means for transmitting, upon transmission of said data, a data phase signal representing a predetermined phase of said data continuously irrespective of transmission of said data, and transmitting said data based on said data phase signal, and reception means for reproducing data reception internal clocks based on said data phase signal and receiving said data according to the reproduced internal clocks.

28. A data transmission system according to claim 27, wherein said first and second devices are a buffer and a DRAM, respectively, the transmission means of said buffer has means for outputting a write data phase signal to said DRAM as said data phase signal, the reception means of said buffer has means for receiving a read data phase signal from said DRAM as said data phase signal, the reception means of said DRAM has means for reproducing said data reception internal clocks from said write data phase signal, and the means for receiving said data according to said reproduced internal clocks, and the transmission means of said DRAM has means for outputting a read data phase signal as said data phase signal at timing relying on said received write data phase signal.

29. A data transmission system according to claim 28, wherein said write data phase signal and said read data phase signal are bidirectionally

transmitted onto the same signal line at mutually different timing.

30. A data transmission system according to claim 28, wherein said write data phase signal and said read data phase signal are bidirectionally transmitted onto mutually different signal lines at mutually different timing.

31. A data transmission system according to claim 28, wherein said read data phase signal reception means of said buffer has means for reproducing data reception buffer internal clocks based on buffer internal clocks and said read data phase signal, and said read data phase signal output means of said DRAM has means for reproducing DRAM internal clocks for outputting said read data phase signal, based on external clocks and said write data phase signal.

32. A memory module having a plurality of memory circuits and a buffer, wherein a command/address signal is transmitted from said buffer to said plurality of memory circuits, and data signals following said command/address signal are transmitted/received between said buffer and said plurality of memory circuits, wherein at least one of said plurality of memory circuits and said buffer has skew absorbing means for absorbing timing skews that are caused to occur between said command/address signal and said data signals in dependency on mounting positions of said memory circuits.

33. A memory module according to claim 32, wherein each of said memory circuits is a DRAM, and said command/address signal is outputted synchronously with buffer clocks outputted from said buffer to said memory circuits.

34. A memory module according to claim 33, wherein said skew absorbing means are provided in said plurality of memory circuits and said buffer, respectively.

35. A memory module according to claim 34, wherein said data signals are transmitted/received between said plurality of DRAMs and said buffer synchronously with data phase signals representing phases of said data

signals.

36. A memory module according to claim 35, wherein said data phase signals are transmitted bidirectionally between said buffer and said DRAMs at timing that avoids collision therebetween, and said DRAMs and said buffer produce internal clocks based on said received data phase signals and perform reception/transmission of data according to said internal clocks.

37. A memory module according to claim 35, wherein said data phase signals are transmitted bidirectionally between said buffer and said DRAMs via mutually different wirings, and said DRAMs and said buffer produce internal clocks based on said received data phase signals and perform reception/transmission of data according to said internal clocks.

38. A memory module according to claim 36, wherein each of said DRAMs is given a command/address signal from said buffer synchronously with said buffer clocks and further given a write data phase signal (WDPS) from said buffer as said data phase signal, and said skew absorbing means of said DRAM has means for producing a plurality of phase clocks for receiving said command/address signal according to said buffer clocks, means for producing data reception DRAM internal phase clocks from said WDPS, and means for domain-crossing said command/address signal received synchronously with said phase clocks, to said data reception DRAM internal phase clocks.

39. A memory module according to claim 38, wherein said DRAM outputs a read data phase signal (RDPS) to said buffer as said data phase signal, and said skew absorbing means of said buffer has means for producing data reception buffer internal phase clocks from said RDPS received from said DRAM, means for producing buffer internal phase clocks based on said WDPS, and means for causing a read data signal inputted synchronously with said RDPS, to match with said buffer internal phase clocks.

40. A memory module according to claim 36, wherein said DRAM is given a write data phase signal (WDPS) from said buffer as said data phase

signal, and inputted with a data signal synchronously with said WDPS, and said skew absorbing means of said DRAM has means for producing data reception DRAM internal phase clocks from said WDPS, means for producing a plurality of phase clocks from said buffer clocks, and means for domain-crossing a data signal received synchronously with said data reception DRAM internal phase clocks, to said plurality of phase clocks.

41. A memory module according to claim 40, wherein said DRAM outputs a read data phase signal (RDPS) based on buffer clocks, and said skew absorbing means of said buffer has means for producing data reception buffer internal phase clocks based on said RDPS, means for producing buffer internal phase clocks based on global clocks, and means for causing a data signal read from said DRAM and received according to said data reception buffer internal phase clocks, to match with said buffer internal phase clocks, thereby to perform domain crossing.

42. A memory module having a plurality of memory circuits and a buffer, wherein a command/address signal is transmitted from said buffer to said plurality of memory circuits, and data signals following said command/address signal are transmitted/received between said buffer and said plurality of memory circuits, wherein said data signals are transmitted/received between said plurality of memory circuits and said buffer synchronously with data phase signals transmitted onto the same signal line alternately from said memory circuits and said buffer, and said buffer has means for outputting a control signal for defining a transmission time of said data phase signal in each of said memory circuits and said buffer.

43. A memory module according to claim 42, wherein said memory circuit comprises a control circuit for controlling transmission of said data phase signal in response to reception of said control signal.

44. A memory module according to claim 42, wherein said buffer controls transmission of said data phase signal to said memory circuit based on

said internally produced control signal.

45. A memory system having a plurality of memory circuits and a control circuit for controlling said plurality of memory circuits according to main clocks, wherein said plurality of memory circuits and said control circuit are connected via first wiring for transmitting/receiving data signals, and second wiring having a length different from that of said first wiring, characterized in that said control circuit attains a clock signal obtained by n-dividing (n is a positive integer equal to or greater than 2) said main clocks in frequency, outputs a command/address signal to said plurality of memory circuits via said second wiring while matching said command/address signal with said n-divided clock signal, and outputs via said first wiring a data phase signal (DPS) having a predetermined frequency relationship with said n-divided clock signal and representing a phase of said data signal, and said plurality of memory circuits each absorb a timing skew caused by a difference in wiring length between said first and second wirings, using said data phase signal.

46. A memory system according to claim 45, wherein each of said memory circuits is a DRAM, and said data phase signal (DPS) has a frequency obtained by n-dividing said main clocks in frequency.

47. A memory system according to claim 46, wherein said control circuit is a buffer mounted on a module along with said DRAMs, and global clocks are fed to said buffer from a memory controller as said main clocks.

48. A memory system according to claim 46, wherein said control circuit is a memory controller directly connected to said DRAMs via said first and second wirings, and said memory controller is given system clocks as said main clocks.

49. A memory system according to claim 46, wherein said control circuit outputs said n-divided clock signal and a command/address signal matched with said clock signal to each DRAM via said second wiring, and further outputs a data phase signal having the same frequency as said clock

signal to each DRAM via said first wiring, and each DRAM causes the command/address signal received from said control circuit synchronously with said clock signal, to match with said received data phase signal, thereby to absorb said timing skew.

50. A memory system according to claim 49, wherein when the command/address signals transferred in a period are m times at maximum, said DRAM receives each command/address signal by one of internal clock signals produced per 1/m phase from timing of said n-divided clock signal.

51. A memory system according to claim 50, wherein said DRAM produces internal data phase clocks at every one of 1/m phase from the timing of said data phase signal received from said control circuit, and produces an internal command/address signal by associating said internal clock signal and said internal data phase clocks with each other and delivering an internal command/address signal to previously associated one of said internal data phase clocks from said internal clock signal.

52. A memory system according to claim 51, wherein said control circuit outputs data signals to be written into said DRAMs, to said DRAMs synchronously with the timing of said data phase signals and, when the data signals transferred in a period are k times at maximum, each data signal is stored into the DRAM according to one of internal clock signals produced at every one of 1/k phase from the timing of said data phase signal transmitted from said control circuit.

53. A memory system according to claim 52, wherein, upon reading a data signal from said DRAM, said DRAM produces a data phase signal (RDPS) based on a data phase signal (WDPS) given from said control circuit, and transmits the read data signal synchronously with timing of said RDPS.

54. A memory system according to claim 53, wherein said control circuit, in response to reception of said RDPS from said DRAM, receives the read data signal according to one of internal clock signals produced at every

one of 1/k phase from the timing of said RDPS, and produces an internal read data signal by associating said internal clock signal and internal clocks internally produced at every one of 1/k phase from the timing of said WDPS produced in said control circuit, and delivering the data signal received by said internal clock signal to previously associated one of said internal clocks.

55. A memory system according to claim 54, wherein said command/address signal is transmitted from said control circuit synchronously with leading and trailing edges of said n-divided clock signal, and received into said DRAM synchronously with leading and trailing edges of said n-divided clock signal.

56. A memory system according to claim 46, wherein said control circuit outputs said n-divided clock signal and a command/address signal matched with said clock signal to each DRAM via said second wiring, and further outputs a data phase signal having the same frequency as said clock signal to each DRAM via said first wiring, and each DRAM causes the data signal received from said control circuit synchronously with said clock signal, to match with said received data phase signal, thereby to absorb said timing skew.

57. A memory system according to claim 56, wherein each DRAM has means for producing internal data phase clocks at every one of 1/m phase from the timing of said data phase signal received from said control circuit, and means for producing internal clocks at every one of 1/m phase from said n-divided clock signal, and produces an internal data signal by associating said internal data phase clocks and said internal clocks with each other, and delivering an internal data signal to previously associated one of said internal clocks from said internal data phase clocks.

58. A memory system according to claim 57, wherein said control circuit receives data signals read from said DROM synchronously with the timing of said data phase signals (RDPS) from said DROM and, when the data signals transferred in a period are k times at maximum, said control circuit

stores the data signals by associating internal data phase clocks produced at every one of 1/k phase from the timing of said RDPS transmitted from said DRAM, and internal phase clocks of said control circuit with each other.

59. A memory system according to claim 45, wherein said data phase signals are transmitted/received between said control circuit and said memory circuit via the same signal line or different signal lines.

60. A memory system according to claim 45, wherein said plurality of DRAMs are mounted on a single module, said control circuit is a memory controller connected to said plurality of DRAMs via first wirings having substantially the same wiring length and via second wiring having a wiring length greater than that of said first wiring, and said memory controller is given system clocks as said main clocks, n-divides said system clocks in frequency to thereby output an n-divided clock signal to each DRAM via said second wiring, and outputs said data phase signal at a frequency equal to that of said clock signal.

61. A memory system according to claim 60, wherein said plurality of DRAMs on said module are divided into a plurality of groups, and each group is applied with said second wiring individually.

62. A memory system according to claim 60, wherein said data phase signal transmitted onto said first wiring has an advanced phase relative to a phase of said n-divided clock signal.

63. A memory system according to claim 60, wherein said plurality of DRAMs on said module are divided into a plurality of groups, and said plurality of groups are commonly applied with said second wiring.

64. A memory system according to claim 63, wherein mutually different phase offset values are given to said data phase signals fed to said plurality of groups.